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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,127	01/20/2004	Joachim Schnabel	INFN/0051	8829

46798 7590 01/10/2006

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EXAMINER	
NGUYEN, DANG T	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 01/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/761,127	SCHNABEL ET AL.	
	Examiner	Art Unit	
	Dang T. Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-18,20 and 21* is/are rejected.

7)☒ Claim(s) *4 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search history*.

DETAILED ACTION

1. This office action is in response to applicant's amendment filed on 11/11/05. Claims 1, 3, 4, 11, 18 and 19 have been amended. Claim 2 has been canceled. Claim 21 has been added. Claims 1 and 3 - 21 are pending in this application. Claims 1, 11, 18 and 21 are independent claims.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, and 3 - 21, are rejected under 35 U.S.C. 103(a) as being unpatentable over Fiscus, Patent No. US 6,714,473 B1 – filed: Nov. 30, 2001 in view of Jeong, Patent No. 5,680,359 – filed: Oct. 21, 1997.

Regarding independent claim 1, Fig. 1 of Fiscus discloses a method for refreshing dynamic memory cells arranged along word lines and bit lines, comprising:

generating a refresh signal [104] to activate a word line to refresh a charge stored in memory cells [106] arranged on the word line (Col. 2, lines 30-51);

monitoring an amount of charge loss of one or more sets of dynamic reference cells [110 and 112] (Col. 5, lines 32-39); and

adjusting a frequency of the refresh signal based on the monitored amount of charge loss (Col. 6 lines 21-41). However, Fiscus fails to disclose wherein the

frequency of the refresh signal is adjusted by dividing a fundamental frequency by a frequency divider value.

Fig. 6 of Jeong discloses a self-refresh period adjustment circuit comprises frequency dividers (Col. 3 lines 25-30 and Abstract, lines 16-22).

It would have been obvious to incorporate a frequency divider as taught by Jeong into refreshing dynamic memory cells of Fiscus to adjust the frequency of the refresh signal. One having ordinary skill in the art would have been motivated to do so because Jeong suggests the desirability of providing a frequency divider for detecting temperature variations thereby securing the safety f data stored in the memory cells and reducing the amount of power consumption at relatively low or normal temperatures (Col. 3 lines 1-4).

Regarding dependent claim 3, Fiscus as applied to claim 1 above disclosed every aspect of applicant's claimed invention except for wherein adjusting the frequency of the refresh signal comprises adjusting the frequency divider value.

Fig. 6 of Jeong discloses a self-refresh period adjustment circuit comprises frequency dividers (Col. 3 lines 25-30 and Abstract, lines 16-22).

It would have been obvious to incorporate a frequency divider as taught by Jeong into refreshing dynamic memory cells of Fiscus to adjust the frequency of the refresh signal. One having ordinary skill in the art would have been motivated to do so because Jeong suggests the desirability of providing a frequency divider for detecting temperature variations thereby securing the safety f data stored in the memory cells and

reducing the amount of power consumption at relatively low or normal temperatures (Col. 3 lines 1-4).

Regarding dependent claim 6, Fig. 4 of Fiscus discloses wherein monitoring the amount of charge loss of the one or more sets of reference cells comprises:

precharging a first set [110] of the reference cells on a first reference word line [WLL] to a first potential value [VLO] (Col. 4, lines 37-51);

Isolating the first set of reference cells from a first common bit line (see Fig. 4);

a known time later, connecting the first set [110] of reference cells [110 and 112] to the first common bit line [V0]; and

comparing a potential on the first common bit line [V0] with a first reference potential [VLO] (Col. 5 lines 39-41).

Regarding dependent claim 7, Fig. 4 of Fiscus discloses further comprising precharging the first common bit line to a center potential (Col. 4, lines 36-40).

Regarding dependent claim 8, Fig. 4 of Fiscus discloses wherein the first reference potential [VLO] is a ground reference.

Regarding dependent claim 9, Fig. 4 of Fiscus discloses precharging a second set [112] of the reference cells on a second reference word line [WLH] to a second potential value [VHI];

isolating the second set of reference cells from a second common bit line (Fig. 4);

a known time later, connecting the second set [112] of reference cells [110 and 112] to the second common bit line [V1]; and

comparing a potential on the second common bit line [V1] with a second reference potential [VHI] (Col. 5 lines 44-46).

Regarding dependent claim 10, Fiscus discloses wherein adjusting the frequency of the refresh signal based on the monitored amount of charge loss comprises:

increasing the frequency of the refresh signal if the potential on the first common bit line exceeds the first reference potential or the second reference potential exceeds the potential on the second common bit line (Col. 1 lines 33-38); and

decreasing the frequency of the refresh signal if the first reference potential exceeds the potential on the first common bit line and the potential on the second common bit line exceeds the second reference potential (Col. 1 lines 21-29).

Regarding independent claim 11, Figs. 1, 2 and 4 of Fiscus disclose a circuit for adjusting a frequency of a refresh signal used to refresh dynamic memory cells, comprising:

a first set [110] of reference cells connectable to a first common bit line [BLL] by activation of a first common word line [WLL];

a second set [112] of reference cells connectable to a second common bit line [BLH] by activation of a second common word line [WLH]; and

a regulating unit [104] configured to monitor an amount of charge loss of the first [110] and second [112] reference cells (Col. 5, lines 32-39) and adjust the frequency of the refresh signal used to refresh the dynamic memory cells based on the monitored amount of charge loss (Col. 6 lines 21-41). However, Fiscus fails to disclose wherein

the frequency of the refresh signal is adjusted by dividing a fundamental frequency by a frequency divider value.

Fig. 6 of Jeong discloses a self-refresh period adjustment circuit comprises frequency dividers (Col. 3 lines 25-30 and Abstract, lines 16-22).

It would have been obvious to incorporate a frequency divider as taught by Jeong into refreshing dynamic memory cells of Fiscus to adjust the frequency of the refresh signal. One having ordinary skill in the art would have been motivated to do so because Jeong suggests the desirability of providing a frequency divider for detecting temperature variations thereby securing the safety f data stored in the memory cells and reducing the amount of power consumption at relatively low or normal temperatures (Col. 3 lines 1-4).

Regarding dependent claim 12, Figs. 1 and 2 of Fiscus discloses wherein the regulating unit [104] is configured to generate one or more control signals [CSL, SET, EGLF, WL] to activate the first and second sets of reference cells [110 and 112] in order to monitor the amount of charge loss of the first and second reference cells [110 and 112] (Col. 5 lines 32-50).

Regarding dependent claim 13, Figs. 1 and 2 of Fiscus disclose wherein the regulating unit [104] is configured to: increase the frequency of the refresh signal if the loss of charge of either the first and second sets of reference cells exceeds a threshold amount; and decrease the frequency of the refresh signal if the loss of charge of both the first and second sets of reference cells does not exceed the threshold amount (Col. 1 lines 21-38).

Regarding dependent claim 14, Fig. 4 of Fiscus discloses wherein the regulating circuit is configured to:

precharge (Col. 4 lines 37-38) the first and second sets of reference cells [110 and 112] to respective first and second potential values [VLO and VHI],

isolating the first [110] and sets of reference cells from the respective first [V0] and second [V1] common bit lines;

a known time later, connect the first and second sets of reference cells [110 and 112] to the respective first and second common bit lines [V0 and V1];

determine the charge loss of the first set [110] of reference cells by comparing [130] a potential on the first common bit line [V0] with a first reference potential [VLO]; and

determine the charge loss of the second set [112] of reference cells by comparing [132] a potential on the second common bit line V1] with a second reference potential [VHI].

Regarding dependent claim 15, Figs. 1 and 4 of Fiscus disclose wherein:

the first potential value is ground [VLO];

the second potential value is above ground [VHI];

the regulating unit [104] is configured to increase the frequency of the refresh signal if the potential on the first common bit line exceeds the first reference potential, the second reference potential exceeds the potential on the second common bit line (Col. 1 lines 33-38), or both; and

the regulating unit [104] is configured to decrease the frequency of the refresh signal if the first reference potential exceeds the potential on the first common bit line and the potential on the second common bit line exceeds the second reference potential (Col. 1 lines 21-29).

Regarding dependent claim 16, Figs. 1 and 4 of Fiscus disclose wherein the regulating circuit [104] is configured to precharge (Col. 4 lines 37-38) the first and second common bit lines [BBL and BLH] to a center potential prior to connecting the first and second sets [110 and 112] of reference cells to the respective first and second common bit lines [V0 and V1].

Regarding dependent claim 17, Fiscus discloses wherein the regulating unit initiates the monitoring of charge loss of the first and second sets of reference cells (Col. 5 lines 32-39) and the adjusting of the frequency of the refresh signal based on one or more word address signals received from a refresh circuit (Col. 6 lines 21-41).

Regarding independent claim 18, Figs. 1, 2 and 4 of Fiscus disclose a memory device, comprising:

a plurality of dynamic memory cells arranged along word lines and bit lines of the device (Fig. 1 [106]);

at least a first set [110] of reference cells arranged around a first common word line (Fig. 1, [110] connect to 106]) and a first common bit line [V0];

a refresh circuit [104] for generating a refresh signal [CSL or SET...] to refresh the dynamic memory cells [106], and

a refresh frequency adjust circuit to adjust a frequency of the refresh signal based on a monitored amount of charge loss of the first set of reference cells (Col. 1 lines 30-47). However, Fiscus fails to disclose wherein the frequency of the refresh signal is adjusted by dividing a fundamental frequency by a frequency divider value.

Fig. 6 of Jeong discloses a self-refresh period adjustment circuit comprises frequency dividers (Col. 3 lines 25-30 and Abstract, lines 16-22).

It would have been obvious to incorporate a frequency divider as taught by Jeong into refreshing dynamic memory cells of Fiscus to adjust the frequency of the refresh signal. One having ordinary skill in the art would have been motivated to do so because Jeong suggests the desirability of providing a frequency divider for detecting temperature variations thereby securing the safety f data stored in the memory cells and reducing the amount of power consumption at relatively low or normal temperatures (Col. 3 lines 1-4).

Regarding dependent claim 20, Figs. 1 and 4 of Fiscus disclose the memory device further comprising:

at least a second set [112] of reference cells arranged around a second common word line [WLH] and a second common bit line [BLH]; and

wherein the refresh frequency adjust circuit is configured to adjust the frequency of the refresh signal based on a monitored amount of charge loss of both the first and second sets of reference cells (Col. 1 lines 30-47).

Regarding independent claim 21, Figs. 1, 2 and 4 of Fiscus disclose a circuit for adjusting a frequency of a refresh signal used to refresh dynamic memory cells, comprising:

a first set [110] of reference cells connectable to a first common bit line [BLL] by activation of a first common word line [WLL];

a regulating circuit [104] configured to: monitor an amount of charge loss of the first [110] reference cells (Col. 5, lines 32-39) and set a divider value on the basis of the amount of charge loss (Col. 6 lines 21-41). However, Fiscus fails to disclose an oscillator configured to output a clock signal at a fundamental frequency and a frequency divider circuit configured to divide the clock signal at the fundamental frequency by the divider value, thereby producing the refresh signal at an adjusted frequency.

Fig. 6 of Jeong discloses an oscillator [30] configured to output signal from frequency divider (Col. 5 lines 43-47); and a frequency divider [31 or 32 or 33] circuit configured to divide the clock signal at the fundamental frequency by divider value, thereby producing the refresh signal at an adjusted frequency (Col. 6 line 63 – Col. 7 line 2).

It would have been obvious to incorporate a frequency divider as taught by Jeong into refreshing dynamic memory cells of Fiscus to adjust the frequency of the refresh signal. One having ordinary skill in the art would have been motivated to do so because Jeong suggests the desirability of providing a frequency divider for detecting temperature variations thereby securing the safety f data stored in the memory cells and

reducing the amount of power consumption at relatively low or normal temperatures (Col. 3 lines 1-4).

Allowable Subject Matter

3. Claims 4 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

With respect to claim 4, the combination as claimed wherein at least the limitation of "increasing the frequency divider if the monitored amount of charge loss falls below a first threshold value and decreasing the frequency divider if the monitored amount of charge loss exceeds a second threshold value" is not disclosed, suggest, or rendered obvious by the prior art of record.

With respect to claim 19, the combination as claimed wherein at least the limitation of "the fundamental frequency of an oscillator circuit by a counter value, the counter value being the frequency divider value" is not disclosed, suggest, or rendered obvious by the prior art of record.

Dependent claim 5 is allowed based on dependent claim 4 above.

Response to Arguments

4. Applicant's arguments filed 11/11/05 with respect to claims 1 and 3 - 21 have been considered but are moot in view of the new ground(s) of rejection.

Prior art

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yoo et al. Patent No. 5,889,719 Date of Patent: Mar. 30, 1999

Higashiho et al. Patent No. US 6,618,310 Date of Patent: Sep. 9, 2003

Contact Information

6. Any inquiry concerning this communication from the examiner should be directed to Dang Nguyen, who can be reached by telephone at (571) 272-1955. Normal contact times are M-F, 8:00 AM - 4:30 PM.

Upon an unsuccessful attempt to contact the examiner, the examiner's supervisor, Richard Elms, may be reached at (571) 272-1869.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is (703) 305-3900. The faxed phone number for organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the Status of an application may be obtained from the patent Application Information Retrieval (PAIR) system. Status information for published

applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC@uspto.gov.

Dang Nguyen 1/6/2006

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